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REMARKS

This is intended as a full and complete response to the Final Office Action dated May 26, 2006, having a shortened statutory period for response set to expire on August 26, 2006. Please reconsider the claims pending in the application for reasons discussed below.

In the specification, paragraph [0001] has been amended to perfect an unintentionally delayed priority claim. Paragraph [0057] has been amended to correct minor editorial error.

Claims 15 and 20 remain pending in the application upon entry of this response. Claims 1-14 and 16-19 have been cancelled by Applicant without prejudice. Claims 15 and 20 have been rewritten in independent form including all the limitations. Applicant asserts that no new matter has been added in this amendment. Reconsideration of the rejected claims is requested for reasons presented below.

Claim Rejections – 35 U.S.C. § 112

Claim 19 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant respectfully requests the rejection be withdrawn in light of the cancelled claim.

Claim Rejections – 35 U.S.C. § 102

Claims 1-20 are rejected under 35 U.S.C. § 102(e) as being clearly anticipated by *Dordi et al* (U.S. Patent Nos. 6,258,220 and 6,635,157, herein '220 and '157) also (U.S. Publ. Nos. 2004/0084301; 2002/0029961). Applicant has amended the specification and concurrently submitted a petition to correct priority, which will give the present application an effective filing date of March 5, 1999. The '220 patent has a priority date of April 8, 1999. The '157 patent cites the '220, filed April 8, 1999, and provisional application No. 60/110,209, filed on November 30, 1998. However, with respect to the claims for the present invention, the '157 can only be considered prior

art as of April 8, 1999 because the provisional application for which it claims priority does not disclose or claim the subject matter of claims 15 and 20 of the present invention. For example, provisional application No. 60/110,209 does not disclose the use of a thermal anneal chamber. Therefore, with respect to the use of a thermal anneal chamber, both the '156 and the '220 patents have an effective filing date of April 8, 1999, which is later than March 5, 1999, the effective filing date of the present application. Thus, the aforementioned references do not qualify as prior art under 35 U.S.C. § 102(e). Withdrawal of the rejection is respectfully requested.

Claims 1-20 are rejected under 35 U.S.C. § 102(e) as being clearly anticipated by *Dordi et al* (U.S. Patent No. 6,267,853). Applicant has amended the specification and concurrently submitted a petition to correct priority, which will give the present application an effective filing date of March 5, 1999. The aforementioned reference cited as prior art by The Examiner has an effective filing date of July 9, 1999, which is later than March 5, 1999, the effective filing date of the present application. Therefore, the aforementioned reference does not qualify as prior art under 35 U.S.C. § 102(e). Withdrawal of the rejection is respectfully requested.

Claims 10, 11, 17 and 18 are rejected under 35 U.S.C. § 102(e) as being clearly anticipated by *Hanson et al* (U.S. 6,091,498), herein *Hanson*. The Examiner asserts that *Hanson* teaches a semiconductor wafer electrochemical deposition system including a mainframe having a wafer transfer robot therein, a loading station disposed in connection with the mainframe with a loading station robot, multiple electrochemical deposition dells and multiple rinse and dry stations for post-deposition treatment of the semiconductor wafer. Withdrawal of the rejection is respectfully requested in light of the cancelled claims.

Claims 17 and 18 are rejected under 35 U.S.C. § 102(e) as being clearly anticipated by *Curtis et al* (U.S. Patent No. 6,264,752), herein *Curtis*. The Examiner asserts that *Curtis* teaches an electrochemical deposition system including a mainframe having a mainframe wafer transfer robot therein, a loading station having cassette receiving areas, two or more electrochemical deposition processing stations and two or more spin-rinse-dry stations. Withdrawal of the rejection is respectfully requested in light of the cancelled claims.

Claim Rejections – 35 U.S.C. § 103

Claims 1 and 4 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Curtis* in view *Uzoh et al* (U.S. Patent No. 6,123,825), herein *Uzoh*. The Examiner asserts that *Curtis* teaches a wafer processing apparatus including a mainframe with a wafer transfer robot, a loading station and multiple processing stations which included electrodeposition cells which would necessarily require an electrolyte fluid supply connected to the cell. The Examiner further states that *Curtis* fails to teach a thermal anneal chamber disposed adjacent the loading station. The Examiner further asserts that *Uzoh* teaches annealing copper electroplated wafers for the purpose of improving grain structure of the electroplated copper. The Applicant respectfully requests withdrawal of the rejection in light of the cancelled claims.

Claims 2, 3 and 5-8 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Curtis* in view of *Uzoh* as applied to claims 1 and 4 above, and further in view of *Moore et al* (U.S. Patent No. 6,151,447), herein *Moore*. The Examiner asserts that *Curtis* and *Uzoh* teach as described above. The Examiner asserts that *Moore* teaches a thermal anneal chamber useful for processing wafers. The Applicant respectfully requests withdrawal of the rejection in light of the cancelled claims.

Claim 9 is rejected under 35 U.S.C. § 103(a) as being unpatentable over *Curtis* in view of *Uzoh* as applied to claims 1 and 4 above, and further in view of *Togawa et al* (U.S. Patent No. 5,830,045), herein *Togawa*, on grounds that *Togawa* teaches using wafer cassettes for a wafer processing apparatus and including a loading station robot for transferring wafers from the loading station to a first processing station. *Togawa* also teaches a wafer orientor for ensuring proper orientation of the wafers. The Applicant respectfully requests withdrawal of the rejection in light of the cancelled claim.

Claims 10, 11, 15 and 17 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Yoshioka et al* (U.S. Patent No. 5,297,910), herein *Yoshioka*, in view of *Bleck et al* (U.S. Patent No. 5,980,706), herein *Bleck*, and *Uzoh* on grounds that *Yoshioka* teaches a system for treatment of semiconductor wafers including a mainframe having a transfer robot therein, a loading station disposed in connection with the mainframe, wherein the loading station included a transfer robot and multiple

processing stations in connection with the mainframe. The Examiner further asserts that *Bleck* teaches processing stations for semiconductor wafers wherein an electrochemical deposition treatment was carried out. The Examiner further asserts that *Uzoh* teaches that it was customary to perform annealing of the copper layer to ensure small grain size of the copper within the layer. The Applicant respectfully traverses the rejection.

Uzoh teaches an electromigration-resistant copper film structure and the process for forming the structure (Abstract). However, while *Uzoh* does teach a process involving an annealing step, it does not suggest *combining* the structure that performs the annealing step with the structure that performs the previous steps. The Examiner admits that *Uzoh* does not even mention positioning the annealing station adjacent, let alone in connection with, the loading station; however, the Examiner asserts that it would have been obvious to place the annealing station at any convenient location with respect to the apparatus. When rejecting claim 15, the Examiner further states that *Uzoh* suggests using a thermal annealing chamber as a post deposition treatment chamber, ignoring the fact that the thermal anneal chambers of the present invention are in connection with the loading station (unlike *Uzoh*). The Examiner makes no showing that the references suggest the desirability of making the combination and is additionally using impermissible hindsight in combining these three references together.

Regarding claim 15, now written in independent form, *Yoshioka*, *Bleck* and *Uzoh*, alone or in combination, do not teach, show or suggest an electro-chemical deposition system, comprising a mainframe having a mainframe wafer transfer robot disposed therein, a loading station disposed in connection with the mainframe, wherein the loading station comprises one or more loading station robots, one or more processing stations disposed in connection with the mainframe, wherein each processing station comprises one or more electrochemical deposition cells, and one or more post deposition treatment chambers disposed in connection with the mainframe, wherein the one or more post deposition treatment chambers comprise one or more rapid thermal anneal chambers, one or more thermal anneal chambers, or a combination thereof, as recited in claim 15. Withdrawal of the rejection is respectfully requested.

Regarding claims 10, 11 and 17, the Applicant respectfully requests withdrawal of the rejection in light of the cancelled claims.

Claims 10-13 and 17-19 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Yoshioka*) in view of *Bleck* and *Shinbara* (U.S. Patent No. 6,155,275), herein *Shinbara*, on grounds that *Yoshioka* and *Bleck* teach as described above. The Examiner further asserts that *Shinbara* teaches the use of a spin-rinse-dry station for cleaning wafers after processing. The Applicant respectfully requests a withdrawal of the rejection in light of the cancelled claims.

Claim 14 is rejected under 35 U.S.C. § 103(a) as being unpatentable over *Yoshioka* in view of *Bleck* and *Uzoh* or *Yoshioka* in view of *Bleck* and *Shinbara* as applied to claim 10 above, and further in view of *Gonzalez-Martin et al* (U.S. Patent No. 6,213,853), herein *Gonzalez-Martin*, on grounds that *Gonzalez-Martin* teaches a transfer robot for use in semiconductor wafer processing that enables the wafer to be flipped from device side-up to device side-down. In light of the cancelled claims, withdrawal of the rejection is respectfully requested.

Claim 16 is rejected under 35 U.S.C. § 103(a) as being unpatentable over *Yoshioka* in view of *Bleck* and *Uzoh* OR *Yoshioka* in view of *Bleck* and *Shinbara* as applied to claim 10 above, and further in view of *Ting et al* (U.S. Patent No. 5,997,712), herein *Ting*, on grounds that *Ting* teaches the use of an electrolyte replenishing system disposed about the mainframe in fluid communication with each of the electrochemical deposition cells. In light of the cancelled claims, withdrawal of the rejection is respectfully requested.

Claim 20 is rejected under 35 U.S.C. § 103(a) as being unpatentable over *Yoshioka* in view of *Bleck* and *Shinbara* as applied to claims 17-19 and further in view of *Uzoh* on grounds that *Yoshioka* in view of *Bleck* and *Shinbara* teach as described above, with *Uzoh* teaching the use of an annealing step to ensure small grain size of the copper within the layer, and *Yoshioka* additionally teaching multiple identical processing stations to allow an increased throughput by parallel processing of wafers at the different stations. The Applicant respectfully traverses the rejection.

As stated *supra*, *Uzoh* teaches an electromigration-resistant copper film structure and the process for forming the structure (Abstract). However, while *Uzoh* does teach a process involving an annealing step, it does not suggest *combining* the

structure that performs the annealing step with the structure that performs the previous steps. The Examiner admits that *Uzoh* does not even mention positioning the annealing station adjacent, let alone in connection with, the loading station; however, the Examiner asserts that it would have been obvious to place the annealing station at any convenient location with respect to the apparatus. When rejecting claim 20, the Examiner states that *Uzoh* suggests using a thermal annealing chamber to ensure small grain size of a copper layer after the formation of the electroplated copper layer on semiconductor wafers, ignoring that the thermal anneal chambers of the present invention are in connection with the loading station (unlike *Uzoh*). The Examiner makes no showing that the references suggest the desirability of making the combination and is additionally using impermissible hindsight in combining these four references together.

Therefore, *Yoshioka*, *Bleck*, *Shinbara* and *Uzoh*, alone or in combination, do not teach, show or suggest an electro-chemical deposition system, comprising a mainframe having a mainframe wafer transfer robots disposed therein, a loading station disposed in connection with the mainframe, wherein the loading station comprises one or more cassette receiving areas, two or more processing stations disposed in connection with the mainframe, wherein each processing station comprises two or more electrochemical deposition cells, and two or more post deposition treatment chambers in connection with the loading station, wherein the two or more post deposition treatment chambers comprise one or more thermal anneal chambers, and two or more spin-rinse-dry modules, and one or more loading station robots transfer wafers between the one or more cassette receiving areas and the two or more post deposition treatment chambers, as recited in claim 20, now written in independent form. Withdrawal of the rejection is respectfully requested.

In conclusion, the references cited by the Examiner, alone or in combination, do not teach, show, or suggest the invention as claimed.

The secondary references made of record are noted. However, it is believed that the secondary references are no more pertinent to the Applicant's disclosure than the primary references cited in the Final Office Action. Therefore, Applicant believes that a detailed discussion of the secondary references is not necessary for a full and complete response to this Final Office Action.

Having addressed all issues set out in the Final Office Action, Applicant respectfully submits that the claims are in condition for allowance and respectfully request that the claims be allowed.

Respectfully submitted,

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